**National Semiconductor**

May 2004

# LMC8101
# Rail-to-Rail Input and Output, 2.7V Op Amp in micro SMD package with Shutdown

## General Description

The LMC8101 is a Rail-to-Rail Input and Output high performance CMOS operational amplifier. The LMC8101 is ideal for low voltage (2.7V to 10V) applications requiring Rail-to-Rail inputs and output. The LMC8101 is supplied in the die sized micro SMD as well as the 8 pin MSOP packages. The micro SMD package requires 75% less board space as compared to the SOT23-5 package. The LMC8101 is an upgrade to the industry standard LMC7101.

The LMC8101 incorporates a simple user controlled methodology for shutdown. This allows ease of use while reducing the total supply current to 1nA typical. This extends battery life where power saving is mandated. The shutdown input threshold can be set relative to either $V^+$ or $V^-$ using the SL pin (see Application Note section for details).

Other enhancements include improved offset voltage limit, three times the output current drive and lower 1/f noise when compared to the industry standard LMC7101 Op Amp. This makes the LMC8101 ideal for use in many battery powered, wireless communication and Industrial applications.
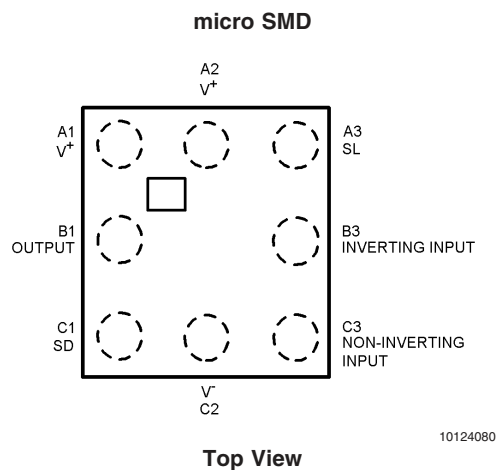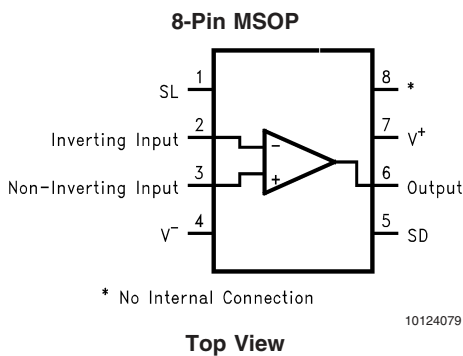
## Features

$V_S$ = 2.7V, $T_A$ = 25˚C, $R_L$ to $V^+$/2, Typical values unless specified.

- Rail-to-Rail Inputs
- Rail-to-Rail Output
  Swing                    Within 35mV of Supplies ($R_L$ =2kΩ)
- Packages Offered:
-    micro SMD package                1.39mm x 1.41mm
-    MSOP package                     3.0mm x 4.9mm
- Low Supply Current              <1mA (max)
- Shutdown Current               1µA (max)
- Versatile Shutdown feature      10µs turn-on
- Output Short Circuit Current     10mA
- Offset Voltage                  ±5 mV (max)
- Gain-Bandwidth                  1MHz
- Supply Voltage Range            2.7V-10V
- THD                            0.18%
- Voltage Noise                  36 $\frac{nV}{\sqrt{Hz}}$

## Applications

- Portable Communication (voice, data)
- Cellular Phone Power Amp Control Loop
- Buffer AMP
- Active Filters
- Battery Sense
- VCO Loop

## Connection Diagrams

**8-Pin MSOP**



* No Internal Connection

10124079

**Top View**

**micro SMD**



10124080

**Top View**

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## Absolute Maximum Ratings (Note 1)

**If Military/Aerospace specified devices are required, please contact the National Semiconductor Sales Office/ Distributors for availability and specifications.**

| | |
|---|---|
| ESD Tolerance | 2KV (Note 2) |
| | 200V (Note 13) |
| $V_{IN}$ differential | ±Supply Voltage |
| Output Short Circuit Duration | (Notes 3, 11) |
| Supply Voltage ($V^+ – V^-$) | 12V |
| Voltage at Input/Output pins | $V^+$ +0.8V, $V^-$ −0.8V |
| Current at Input Pin | ±10mA |
| Current at Output Pin (Notes 3, 12) | ±80mA |
| Current at Power Supply pins | ±80mA |
| Storage Temperature Range | −65˚C to +150˚C |
| Junction Temperature(Note 4) | +150˚C |
| Soldering Information | |
| Infrared or Convection (20 sec.) | 235˚C |
| Wave Soldering (10 sec.) | 260˚C |

## Operating Ratings (Note 1)

| | |
|---|---|
| Supply Voltage ($V^+$ - $V^-$) | 2.7V to 10V |
| Junction Temperature Range (Note 4) | −40˚C to +85˚C |
| Package Thermal Resistance ($\theta_{JA}$) (Note 4) | |
| micro SMD | 220˚C/W |
| MSOP pkg. 8 pin Surface Mount | 230˚C/W |

## 2.7V Electrical Characteristics

Unless otherwise specified, all limits guaranteed for $T_J$ = 25˚C, $V^+$ = 2.7V, $V^-$ = 0V, $V_{CM}$ = $V_O$ = $V^+$/2 and $R_L$ > 1 MΩ to $V^+$/2. **Boldface** limits apply at the temperature extremes.

| Symbol | Parameter | Conditions | Typ (Note 5) | Limit (Note 6) | Units |
|---|---|---|---|---|---|
| $V_{OS}$ | Input Offset Voltage | | ±0.70 | ±5 **±7** | mV max |
| $TCV_{OS}$ | Input Offset Voltage Average Drift | | 4 | | µV/˚C |
| $I_B$ | Input Bias Current | (Note 7) | ±1 | **±64** | pA max |
| $I_{OS}$ | Input Offset Current | | 0.5 | **32** | pA max |
| $R_{in\ CM}$ | Input Common Mode Resistance | | 10 | | GΩ |
| $C_{in\ CM}$ | Input Common Mode Capacitance | | 10 | | pF |
| CMRR | Common Mode Rejection Ratio | 0V < = $V_{CM}$ < = 2.7V | 78 | 60 | dB min |
| | | $V_S$ = 3V 0V < = $V_{CM}$ < = 3V | 78 | 64 **60** | |
| PSRR | Power Supply Rejection Ratio | $V_S$ = 2.7V to 3V | 57 | 50 **48** | dB min |
| CMVR | Input Common-Mode Voltage Range | $V_S$ = 2.7V CMRR > = 50dB | 0.0 | 0.0 | V max |
| | | | 3.0 | 2.7 | V min |
| | | $V_S$ = 3V CMRR > = 50dB | −0.2 | −0.1 | V max |
| | | | 3.2 | 3.1 | V min |

## 2.7V Electrical Characteristics (Continued)

Unless otherwise specified, all limits guaranteed for $T_J = 25°C$, $V^+ = 2.7V$, $V^- = 0V$, $V_{CM} = V_O = V^+/2$ and $R_L > 1$ MΩ to $V^+/2$. **Boldface** limits apply at the temperature extremes.

| Symbol | Parameter | Conditions | Typ (Note 5) | Limit (Note 6) | Units |
|---|---|---|---|---|---|
| $A_{VOL}$ | Large Signal Voltage Gain | Sourcing<br>$R_L = 2kΩ$ to $V^+/2$<br>$V_O = 1.35V$ to $2.45V$ | 3162 | 1000<br>562 | V/V<br>min |
| | | Sinking<br>$R_L = 2kΩ$ to $V^+/2$<br>$V_O = 1.35V$ to $0.25V$ | 3162 | 804<br>**562** | |
| | | Sourcing<br>$R_L = 10kΩ$ to $V^+/2$<br>$V_O = 1.35V$ to $2.65V$ | 4000 | 1778<br>**1000** | V/V<br>min |
| | | Sinking<br>$R_L = 10kΩ$ to $V^+/2$<br>$V_O = 1.35V$ to $0.05V$ | 4000 | 1778<br>**1000** | |
| $V_O$ | Output Swing<br>High | $R_L = 2kΩ$ to $V^+/2$<br>$V_{ID} = 100mV$ | 2.67 | 2.64<br>**2.62** | V<br>min |
| | | $R_L = 10kΩ$ to $V^+/2$<br>$V_{ID} = 100mV$ | 2.69 | 2.68<br>**2.67** | V<br>min |
| | Output Swing<br>Low | $R_L = 2kΩ$ to $V^+/2$<br>$V_{ID} = -100mV$ | 32 | 100<br>**150** | mV<br>max |
| | | $R_L = 10kΩ$ to $V^+/2$<br>$V_{ID} = -100mV$ | 10 | 30<br>**70** | mV<br>max |
| $I_{SC}$ | Output Short Circuit Current | Sourcing to $V^+/2$<br>$V_{ID} = 100mV$ (Note 11) | 20 | 14<br>**6** | mA<br>min |
| | | Sinking to $V^+/2$<br>$V_{ID} = -100mV$ (Note 11) | 10 | 5<br>**4** | mA<br>min |
| $I_S$ | Supply Current | No load, normal operation | 0.70 | 1.0<br>**1.2** | mA<br>max |
| | | Shutdown mode | 0.001 | 1 | µA<br>max |
| $T_{on}$ | Shutdown Turn-on time | (Note 9) | 10 | 15 | µs |
| $T_{off}$ | Shutdown Turn-off time | (Note 9) | 1 | | µs |
| $I_{in}$ | "SL" and "SD" Input Current | | ±1 | **±64** | pA<br>max |
| SR | Slew Rate (Note 8) | $A_V = +1$, $R_L = 10kΩ$ to $V^+/2$<br>$V_I = 1V_{PP}$ | 1 | 0.8 | V/µs<br>min |
| $f_u$ | Unity Gain-Bandwidth | $V_I = 10mV$, $R_L = 2kΩ$ to $V^+/2$ | 750 | | KHz |
| GBW | Gain Bandwidth Product | $f = 100KHz$ | 1 | | MHz |
| $e_n$ | Input-Referred Voltage Noise | $f = 10KHz$, $R_S = 50Ω$ | 36 | | $\frac{nV}{\sqrt{Hz}}$ |
| $i_n$ | Input-Referred Current Noise | $f = 10KHz$ | 1.5 | | $\frac{fA}{\sqrt{Hz}}$ |
| THD | Total Harmonic Distortion | $f = 1KHz$, $AV = +1$,<br>$V_O = 2.2Vpp$,<br>$R_L = 600Ω$ to $V^+/2$ | 0.18 | | % |

# ±5V Electrical Characteristics

Unless otherwise specified, all limits guaranteed for $T_J$ = 25˚C, $V^+$ =5V, $V^-$ = −5V, $V_{CM}$ = $V_O$ = 0V, and $R_L$ > 1 MΩ to gnd. **Boldface** limits apply at the temperature extremes.

| Symbol | Parameter | Conditions | Typ (Note 5) | Limit (Note 6) | Units |
|--------|-----------|------------|-----|-------|-------|
| $V_{OS}$ | Input Offset Voltage | | ±0.7 | ±5 **±7** | mV max |
| $TCV_{os}$ | Input Offset Voltage Average Drift | | 4 | | µV/˚C |
| $I_B$ | Input Bias Current | (Note 7) | ±1 | **±64** | pA max |
| $I_{OS}$ | Input Offset Current | | 0.5 | **32** | pA max |
| $R_{in\ CM}$ | Input Common Mode Resistance | | 10 | | GΩ |
| $C_{in\ CM}$ | Input Common Mode Capacitance | | 10 | | pF |
| CMRR | Common-Mode Rejection Ratio | −5V < = $V_{CM}$ < = 5V | 87 | 70 **67** | dB min |
| PSRR | Power Supply Rejection Ratio | $V_S$ = 5V to 10V | 80 | 76 **72** | dB min |
| CMVR | Input Common-Mode Voltage Range | CMRR ≥ 50 dB | −5.3 | −5.2 **−5.0** | V max |
| | | | 5.3 | 5.2 **5.0** | V min |
| $A_{VOL}$ | Large Signal Voltage Gain | Sourcing $R_L$ = 600Ω $V_O$ = 0V to 4V | 34.5 | 17.8 **10** | V/mV min |
| | | Sinking $R_L$ = 600Ω $V_O$ = 0V to −4V | 34.5 | 17.8 **3.16** | |
| | | Sourcing $R_L$ = 2kΩ $V_O$ = 0V to 4.6V | 138 | 31.6 **17.8** | V/mV min |
| | | Sinking $R_L$ = 2kΩ $V_O$ = 0V to −4.6V | 138 | 31.6 **10** | |
| $V_O$ | Output Swing High | $R_L$ = 600Ω $V_{ID}$ = 100mV | 4.73 | 4.60 **4.54** | V min |
| | | $R_L$ = 2kΩ $V_{ID}$ = 100mV | 4.90 | 4.85 **4.83** | V min |
| | Output Swing Low | $R_L$ = 600Ω $V_{ID}$ = −100mV | −4.85 | −4.75 **−4.65** | V max |
| | | $R_L$ = 2kΩ $V_{ID}$ = −100mV | −4.95 | 4.90 **−4.84** | V max |
| $I_{SC}$ | Output Short Circuit Current | Sourcing, $V_{ID}$ = 100mV (Note 3),(Note 11) | 49 | 30 **25** | mA min |
| | | Sinking, $V_{ID}$ = −100mV (Note 3),(Note 11) | 90 | 60 **52** | mA min |
| $I_S$ | Supply Current | No load, normal operation | 1.1 | 1.7 **1.9** | mA max |
| | | Shutdown mode | 0.001 | 1 | µA |
| $T_{on}$ | Shutdown Turn-on time | (Note 9) | 10 | 15 | µs |
| $T_{off}$ | Shutdown Turn-off time | (Note 9) | 1 | | µs |
| $I_{in}$ | "SL" and "SD" Input Current | | ±1 | **±64** | pA max |

## ±5V Electrical Characteristics (Continued)

Unless otherwise specified, all limits guaranteed for $T_J$ = 25°C, $V^+$ =5V, $V^-$ = –5V, $V_{CM}$ = $V_O$ = 0V, and $R_L$ > 1 MΩ to gnd. **Boldface** limits apply at the temperature extremes.

| Symbol | Parameter | Conditions | Typ (Note 5) | Limit (Note 6) | Units |
|---|---|---|---|---|---|
| SR | Slew Rate (Note 8) | $A_V$ = +10, $R_L$ = 10kΩ, $V_O$ = 10Vpp, $C_L$ = 1000pF | 1.2 | | V/μs |
| $f_u$ | Unity Gain-Bandwidth | $V_I$ = 10mV, $R_L$ = 2kΩ | 840 | | KHz |
| GBW | Gain Bandwidth Product | f = 10KHz | 1.3 | | MHz |
| $e_n$ | Input-Referred Voltage Noise | f = 10KHz, $R_s$ = 50Ω | 33 | | $\frac{nV}{\sqrt{Hz}}$ |
| $i_n$ | Input-Referred Current Noise | f = 10KHz | 1.5 | | $\frac{fA}{\sqrt{Hz}}$ |
| THD | Total Harmonic Distortion | f = 10KHz, AV = +1, $V_O$ =8Vpp, $R_L$ = 600Ω | 0.2 | | % |

**Note 1:** Absolute Maximum Ratings indicate limits beyond which damage to the device may occur. Operating Ratings indicate conditions for which the device is intended to be functional, but specific performance is not guaranteed. For guaranteed specifications and the test conditions, see the Electrical Characteristics.

**Note 2:** Human body model, 1.5kΩ in series with 100pF.

**Note 3:** Applies to both single-supply and split-supply operation. Continuous short circuit operation at elevated ambient temperature can result in exceeding the maximum allowed junction temperature at 150°C. Output currents in excess of 40mA over long term may adversely affect reliability.

**Note 4:** The maximum power dissipation is a function of $T_{J(MAX)}$, $θ_{JA}$ and $T_A$. The maximum allowable power dissipation at any ambient temperature is $P_D$ = ($T_{J(MAX)}$ – $T_A$)/$θ_{JA}$. All numbers apply for packages soldered directly onto a PC board.

**Note 5:** Typical Values represent the most likely parametric norm.

**Note 6:** All limits are guaranteed by testing or statistical analysis.

**Note 7:** Positive current corresponds to current flowing into the device.

**Note 8:** Slew rate is the slower of the rising and falling slew rates.

**Note 9:** Shutdown Turn-on and Turn-off times are defined as the time required for the output to reach 90% and 10%, respectively, of its final peak to peak swing when set for Rail to Rail output swing with a 100KHz sine wave, 2KΩ load, and $A_V$ = +10.

**Note 10:** Limiting input pin current is only necessary for input voltages that exceed absolute maximum input voltage ratings.
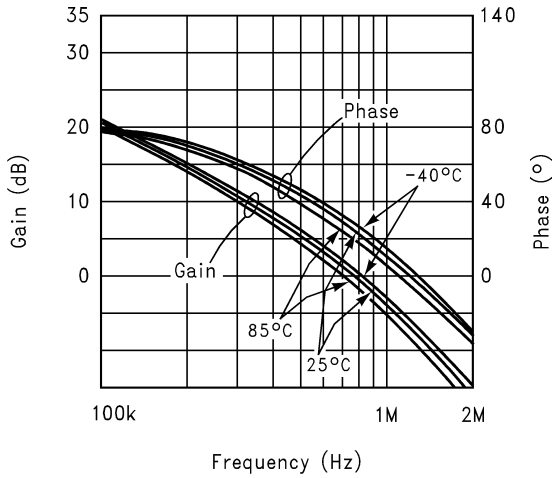
**Note 11:** Short circuit test is a momentary test. See Note 12.

**Note 12:** Output short circuit duration is infinite for $V_S$ < 6V. Otherwise, extended period output short circuit may damage the device.
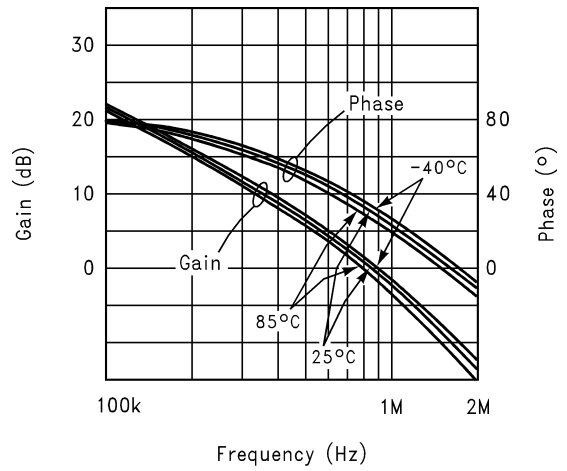
**Note 13:** machine Model, 0Ω in series with 200pF.

# Typical Performance Characteristics $V_S$ = 2.7V, Single Supply, $V_{CM}$ = $V^+$/2, $T_A$ = 25˚C unless specified

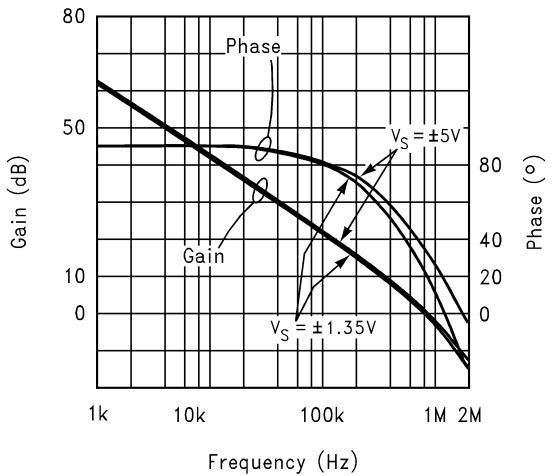**Gain/Phase vs. Frequency ($R_L$ = 2k, $V_S$ = ± 1.35V)**



10124002

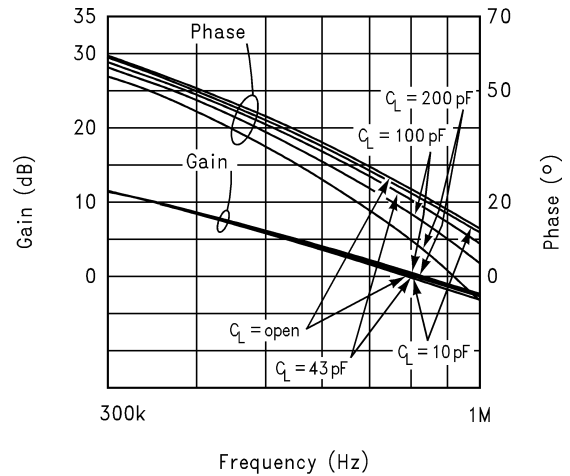**Gain/Phase vs. Frequency ($R_L$ = 2k, $V_S$ = ± 5V)**



10124001
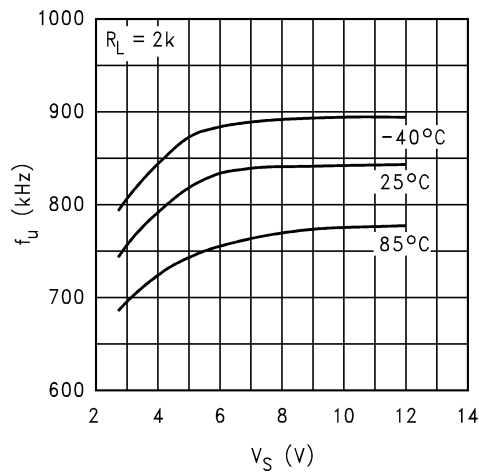
**Gain/Phase vs. Frequency ($R_L$ = Open)**



10124004

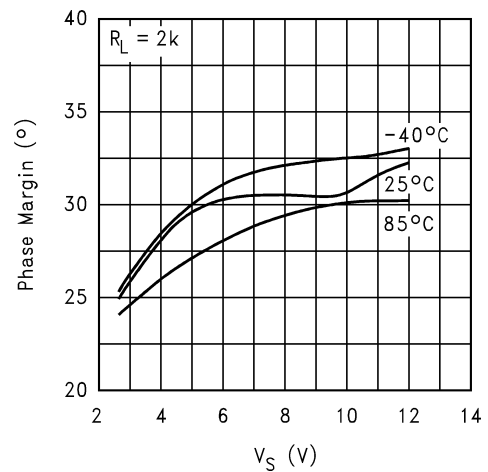**Gain vs. Phase for various $C_L$**
**$V_S$ = ±1.35V**



10124003
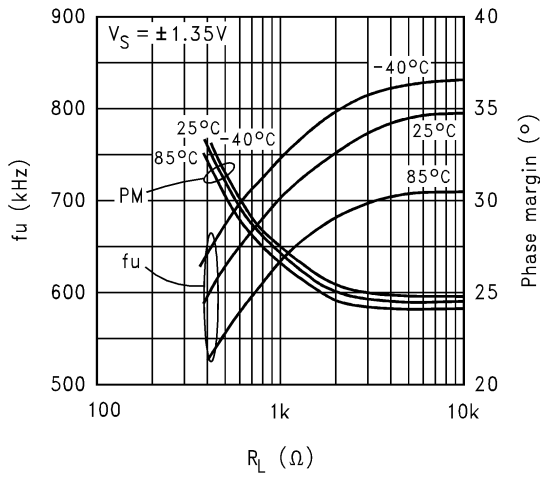
**Unity Gain Frequency vs. Supply Voltage**
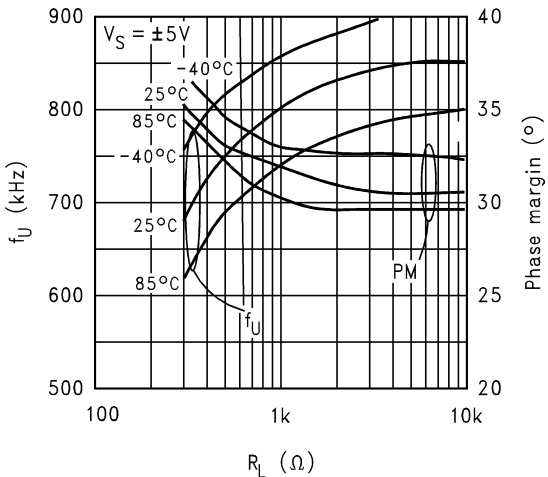


10124005

**Phase Margin vs. Supply Voltage**



10124006

# Typical Performance Characteristics $V_S$ = 2.7V, Single Supply, $V_{CM}$ = V$^+$/2, $T_A$ = 25˚C unless specified (Continued)

### Unity Gain Frequency and Phase Margin vs. Load



10124007
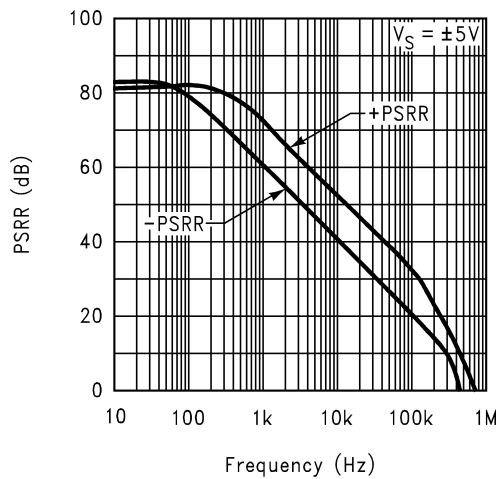
### Unity Gain Frequency and Phase Margin vs. Load



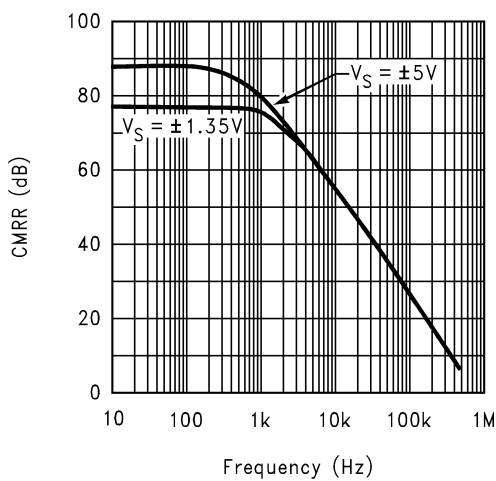10124008

### PSRR vs. Frequency
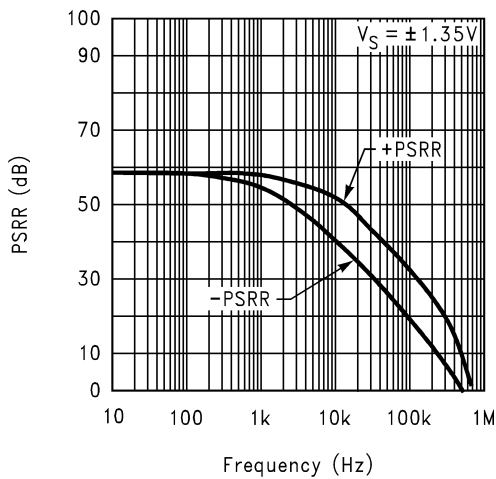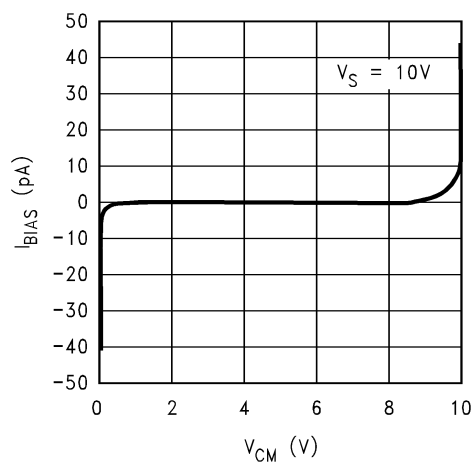


10124010

### PSRR vs. Frequency



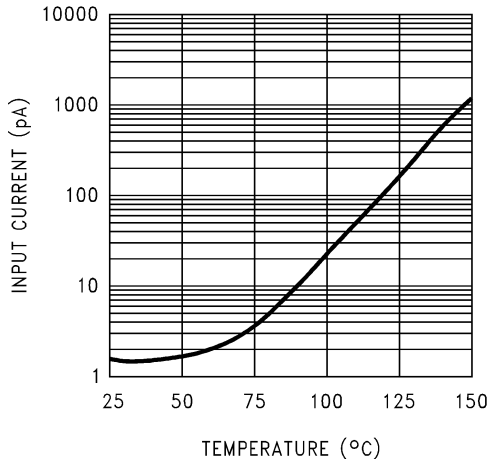10124009

### CMRR vs. Frequency



10124011

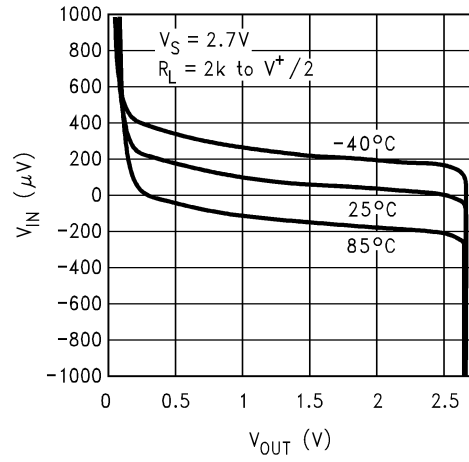### Input Bias Current vs. Common Mode Voltage @ 85˚C



10124013

# Typical Performance Characteristics $V_S$ = 2.7V, Single Supply, $V_{CM}$ = V$^+$/2, $T_A$ = 25˚C unless specified (Continued)
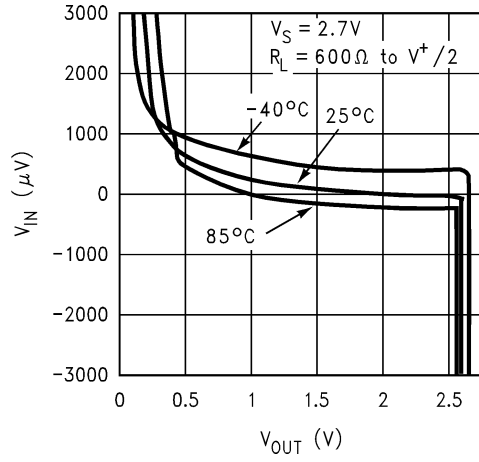
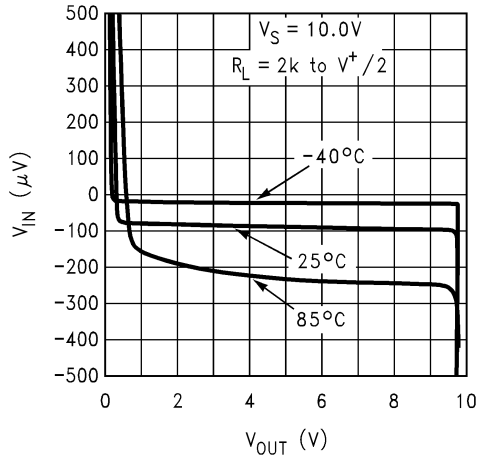**Input Current vs. Temperature**
**$V_S$ = 10V**
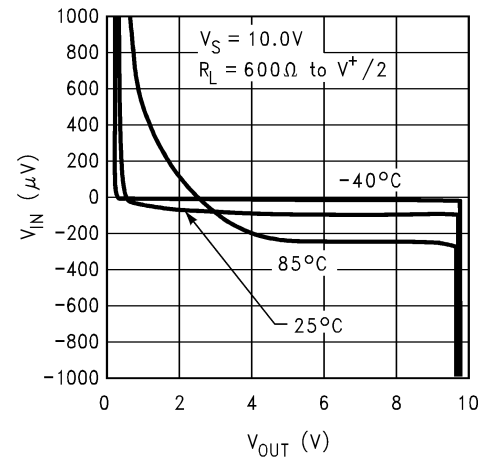
10124091

**$V_{IN}$ vs. $V_{OUT}$**

10124023

**$V_{IN}$ vs. $V_{OUT}$**

10124083

**$V_{IN}$ vs. $V_{OUT}$**

10124028

**$V_{IN}$ vs. $V_{OUT}$**

10124024

**Supply Current vs. Supply Voltage**

10124029

## Typical Performance Characteristics $V_S$ = 2.7V, Single Supply, $V_{CM}$ = V+/2, $T_A$ = 25˚C unless specified (Continued)

**Delta $V_{OS}$ vs. $V_{CM}$
(Ref $V_{CM}$ = 1.35V)**



10124092

**Delta $V_{OS}$ vs. $V_{CM}$
(Ref $V_{CM}$ = 5V)**



10124093

**Offset Voltage vs. $V_{SUPPLY}$**



10124037

**Output Positive Swing vs. Supply Voltage
$R_L$ = 600$\Omega$ to V+/2**



10124025

**Output Positive Swing vs. Supply Voltage
$R_L$ = 2k to V+/2**



10124027

**Output Negative Swing vs. Supply Voltage
$R_L$ = 600$\Omega$ to V+/2**



10124035

# Typical Performance Characteristics $V_S$ = 2.7V, Single Supply, $V_{CM}$ = V+/2, $T_A$ = 25˚C unless specified (Continued)

**Output Negative Swing vs. Supply Voltage, $R_L$ = 2k to V+/2**

10124036

**Short Circuit Sinking Current vs. Supply Voltage**

10124026
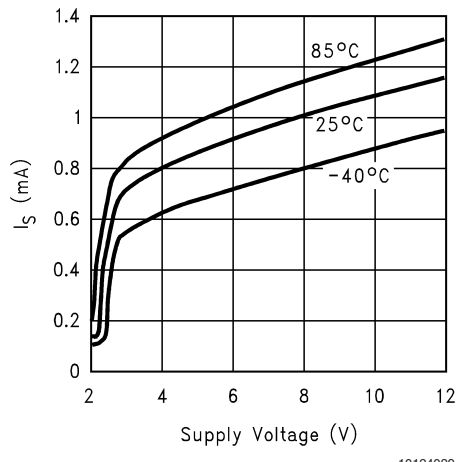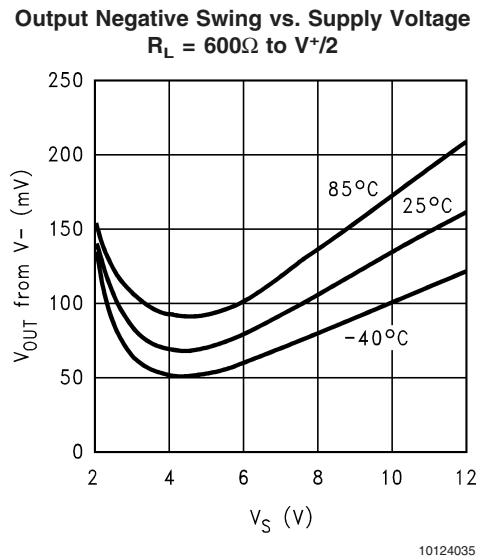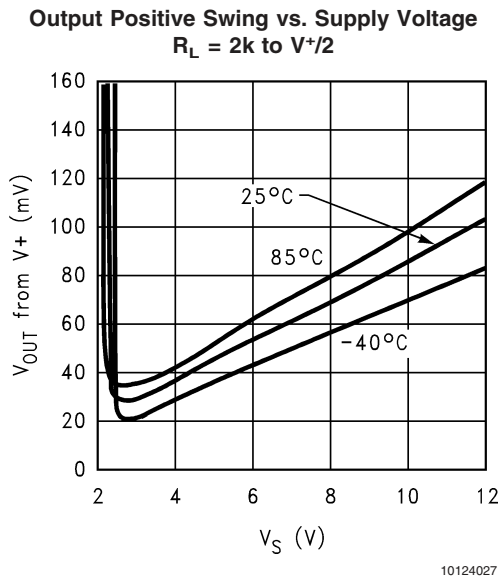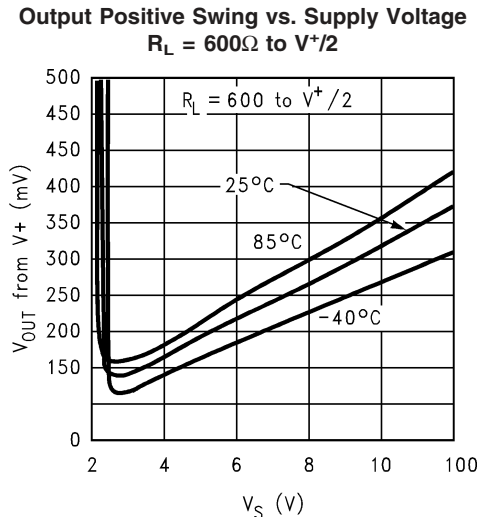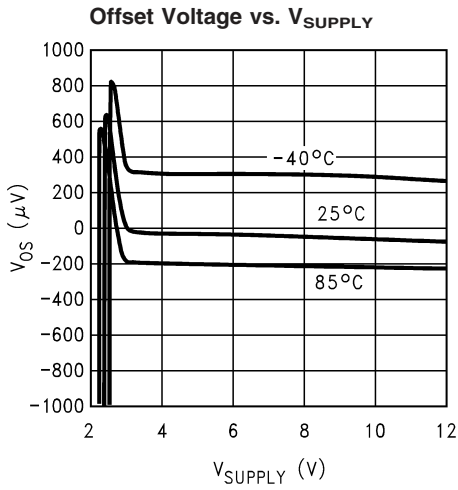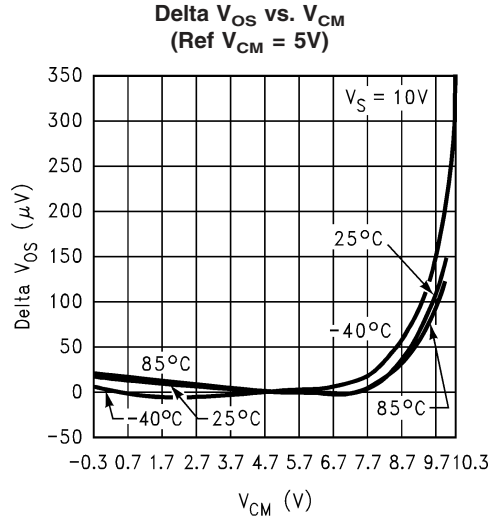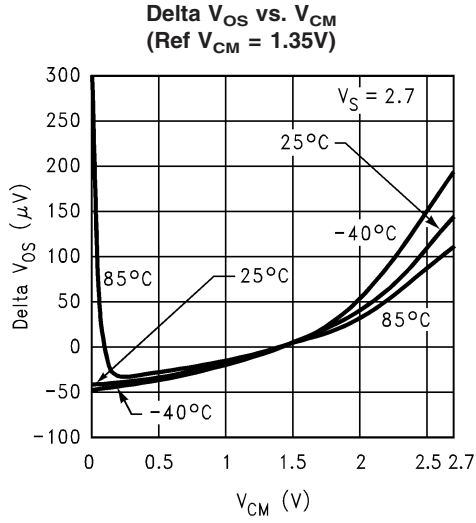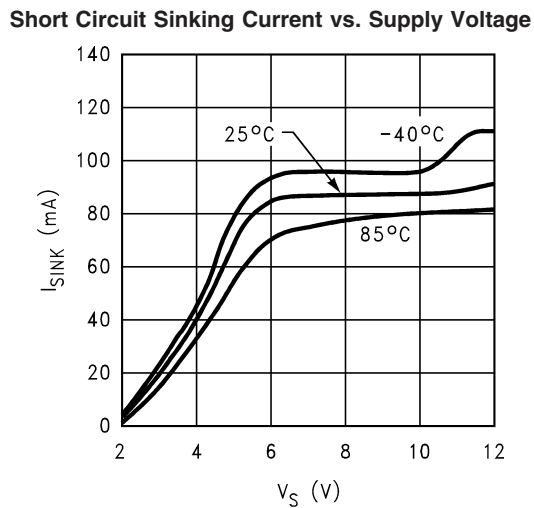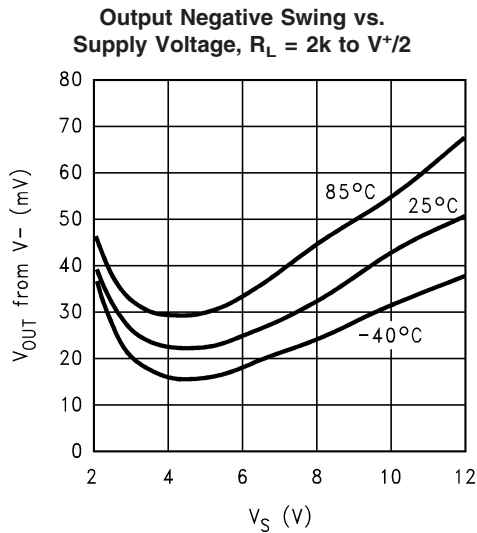
**Short Circuit Sourcing Current vs. Supply Voltage**

10124030

**Undistorted Output Voltage Swing vs. Output Load Resistance**
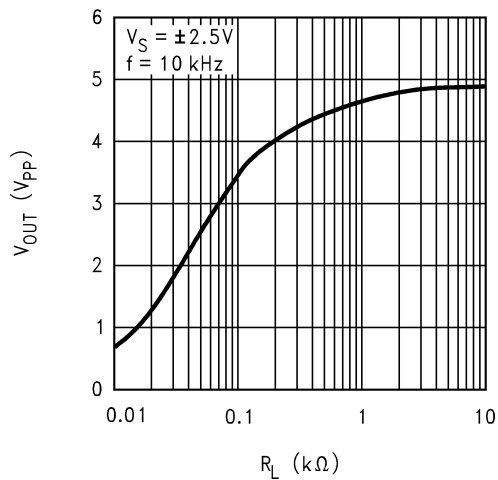
10124046

**Step Response 1% settling time and % overshoot vs. Cap Load**
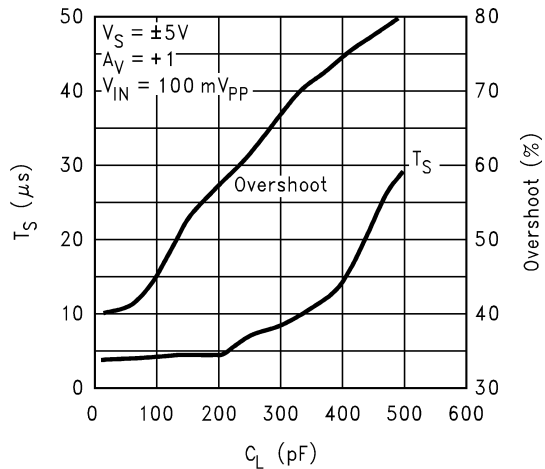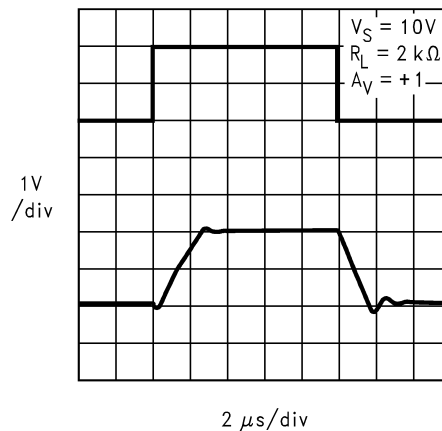
10124014

**Large Signal Step Response**

10124015

# Typical Performance Characteristics $V_S$ = 2.7V, Single Supply, $V_{CM}$ = V⁺/2, $T_A$ = 25°C unless specified (Continued)

**Small Signal Step Response**

$V_S$ = 10V
$R_L$ = 2 kΩ
$A_V$ = +10

50 mV
/div

2 μs/div
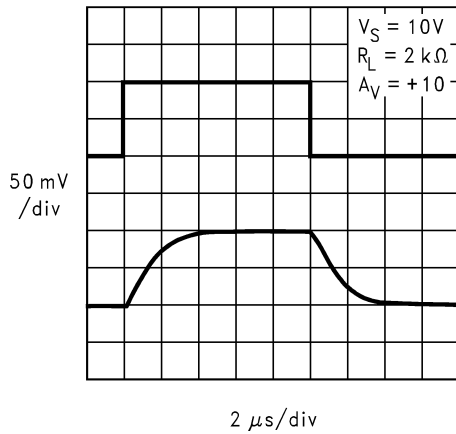
10124016

**Large Signal Step Response**

$V_S$ = 10V
$R_L$ = 2 kΩ
$A_V$ = +10
$C_L$ = 1000 pF

1V
/div

2 μs/div
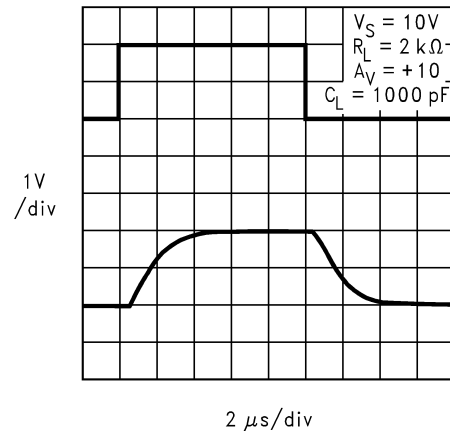
10124017

**Small Signal Step Response**

$V_S$ = 10V
$R_L$ = 2k
$A_V$ = +1

50 mV
/div

2 μs/div
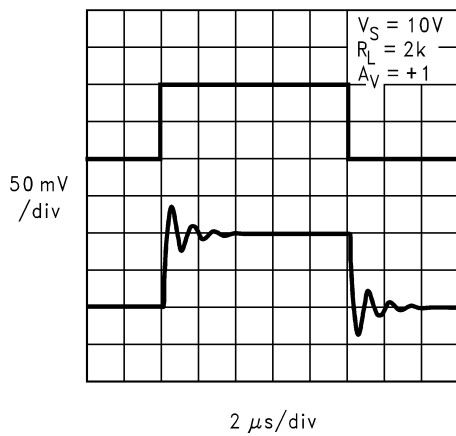
10124018

**Small Signal Step Response**

$V_S$ = 10V
$R_L$ = 2 kΩ
$A_V$ = +10
$C_L$ = 1000 pF

50 mV
/div

2 μs/div
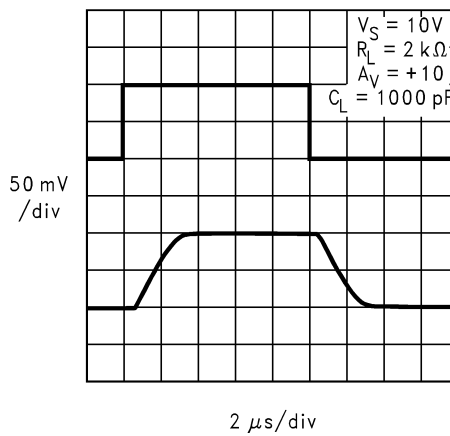
10124019

**Large Signal Step Response**

$V_S$ = 10V
$R_L$ = 2 kΩ
$A_V$ = +10

1V
/div

2 μs/div
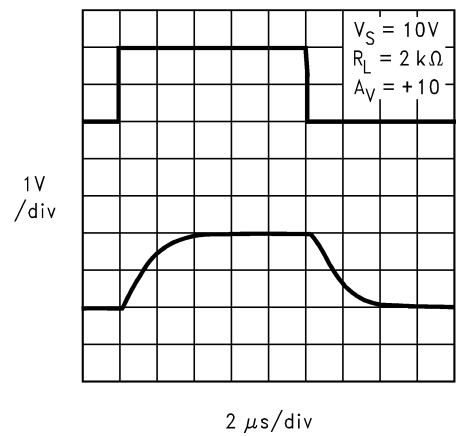
10124020

**Large Signal Step Response**

$V_S$ = 10V
$R_L$ = 2 kΩ
$A_V$ = +1
$C_L$ = 200 pF

1V
/div

2 μs/div
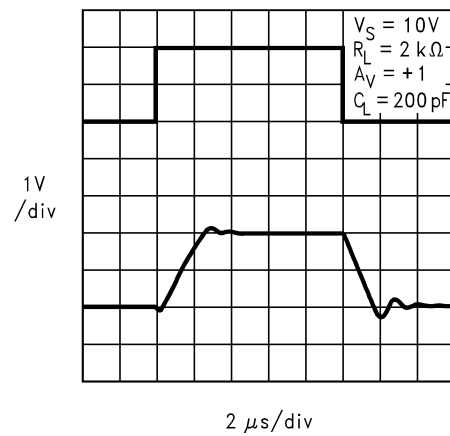
10124021

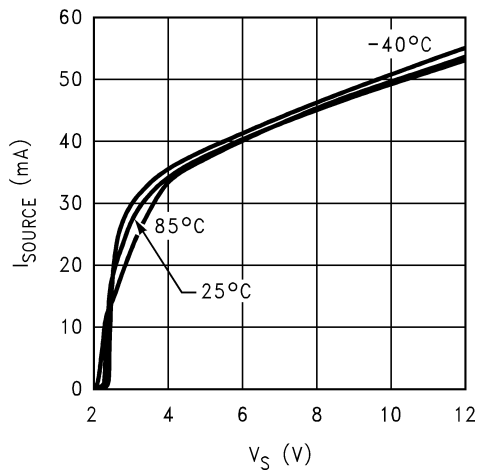# Typical Performance Characteristics $V_S$ = 2.7V, Single Supply, $V_{CM}$ = V$^+$/2, $T_A$ = 25°C unless specified (Continued)

**Small Signal Step Response**

$V_S$ = 10V
$R_L$ = 2 k$\Omega$
$A_V$ = + 1
$C_L$ = 200 pF

50 mV/div

2 $\mu$s/div
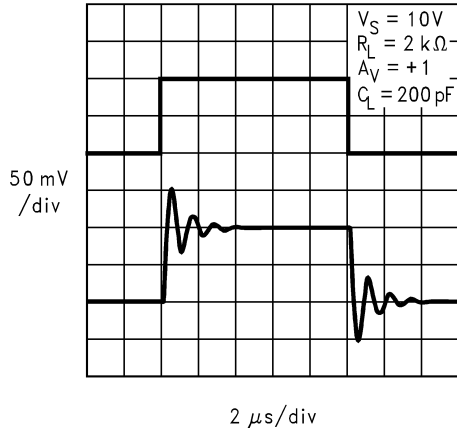
10124022

**Slew Rate vs. Supply Voltage**

Negative

$A_V$ = + 1
$V_{OUT}$ = 2V$_{P-P}$
$R_L$ = 10k to V$^+$/2
$C_L$ = 20 pF

Positive

10124038

**Slew Rate vs. Capacitive Load**

Positive
Negative
Average

$V_S$ = +10V
$A_V$ = +10
$V_O$ = 10V$_{P-P}$
$R_F$ = 10k
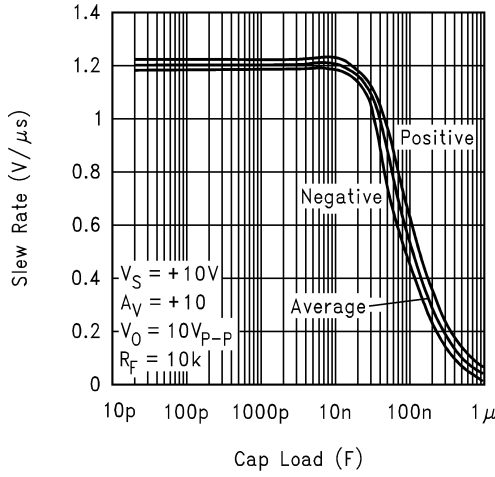
10124039

**Slew Rate vs. Capacitive Load**

Positive
Negative
Average

$V_S$ = +5V
$A_V$ = +10
$V_O$ = 4V$_{PP}$
$R_F$ = 10k
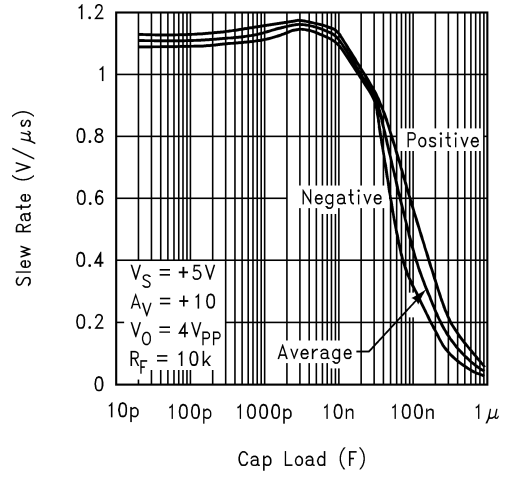
10124041

**Slew Rate vs. Capacitive Load**

Positive
Average
Negative
Negative
Average
Positive

$V_S$ = +2.7V
$A_V$ = +10
$V_O$ = 2V$_{PP}$
$R_F$ = 10k
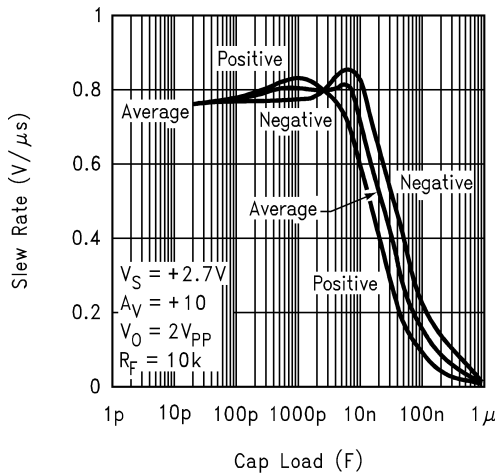
10124042

**Slew Rate vs. Capacitive Load**

$A_V$ = +10
$R_F$ = 10k
$V_S$ = 10
$V_S$ = 5V
$V_S$ = 2.7
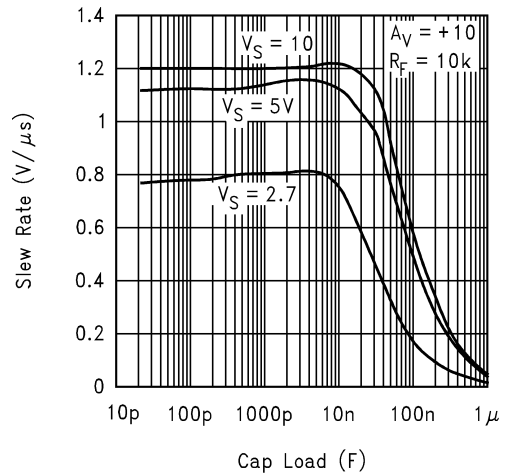
10124043

## Typical Performance Characteristics $V_S$ = 2.7V, Single Supply, $V_{CM}$ = $V^+$/2, $T_A$ = 25˚C unless specified (Continued)

**Voltage Noise vs. Frequency**

$A_V$ = +10
$R_F$ = 10k
$V_{CM}$ = $V^+$/2

$V_S$ = 2.7V
$V_S$ = 5V
$V_S$ = 10V

$e_n$ (nV/$\sqrt{Hz}$)

Frequency (Hz)

10124040

**Voltage Noise vs. $V_{CM}$ @ Various Frequencies**

$V_S$ = ±5V

10 Hz
100 Hz
1 kHz
100 kHz
10 kHz

$e_n$ (nV/$\sqrt{Hz}$)

$V_{CM}$ (V)

10124012

**THD+N vs. Amplitude**

$V_S$ = ±5V
$A_V$ = +1
f = 10 kHz

150 Ω
600 Ω
100 kΩ

THD+N (%)

$V_{IN}$ ($V_{PP}$)

10124044

**THD+N vs. Frequency**

$V_S$ = ±5V
$A_V$ = +1
$V_{IN}$ = 3$V_{PP}$
$R_L$ = 100 kΩ

THD+N (%)

Frequency (Hz)

10124045

**Sourcing Current vs. Output Voltage ($V_S$ = 2.7V)**

−40°C
85°C
25°C

Output Current (mA)

Output Voltage (V) Ref to V+

10124087

**Sinking Current vs. Output Voltage ($V_S$ = 2.7V)**

−40°C
85°C
25°C

Output Current (mA)

Output Voltage (V) $R_{REF}$ to V−
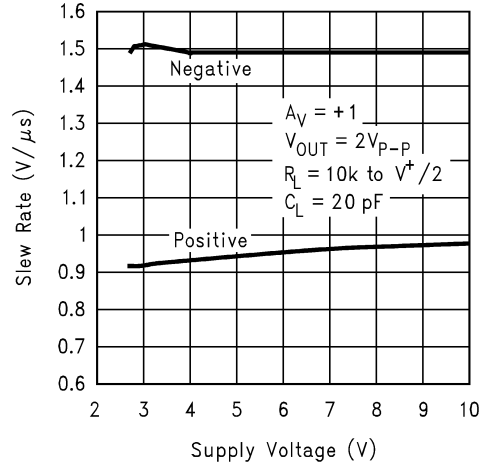
10124085

# Typical Performance Characteristics $V_S$ = 2.7V, Single Supply, $V_{CM}$ = $V^+$/2, $T_A$ = 25˚C unless specified (Continued)

**Sourcing Current vs. Output Voltage ($V_S$ = 10V)**



10124086

**Sinking Current vs. Output Voltage ($V_S$ = 10V)**



10124084

**Cap Load vs. $I_{OUT}$**



10124088
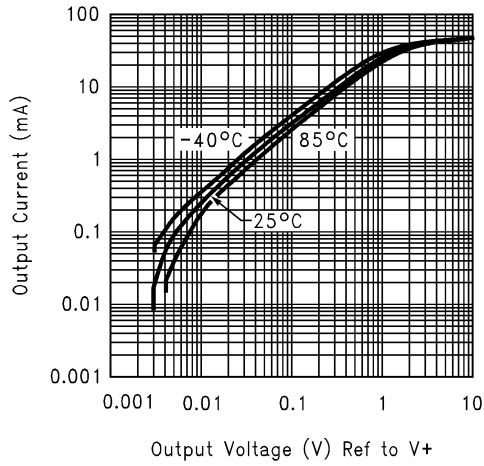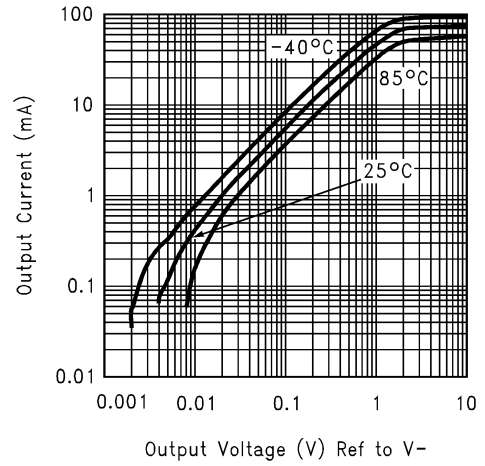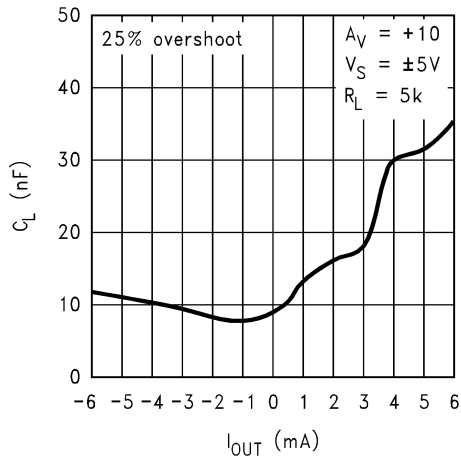
**Cap Load vs. Isolation Resistance**



10124090

14
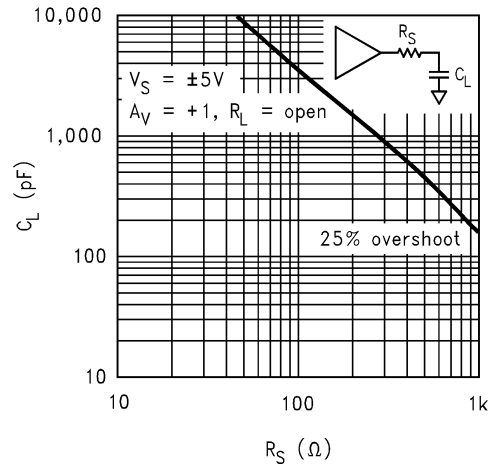
# Application Notes

## SHUTDOWN FEATURES

The LMC8101 is capable of being turned off in order to conserve power. Once in shutdown, the device supply current is drastically reduced (1µA maximum) and the output will be "Tri-stated".

The shutdown feature of the LMC8101 is designed for flexibility. The threshold level of the SD input can be referenced to either V⁻ or V⁺ by setting the level on the SL input. When the SL input is connected to V⁻, the SD threshold level is referenced to V⁻ and vice versa. This threshold will be about 1.5V from the supply tied to the SL pin. So, for this example, the device will be in shutdown as long as the SD pin voltage is within 1V of V⁻. In order to ensure that the device would not "chatter" between active and shutdown states, hysteresis is built into the SD pin transition (see *Figure 1* for an illustration of this feature). The shutdown threshold and hysteresis level are independent of the supply voltage. *Figure 1* illustration applies equally well to the case when SL is tied to V⁺ and the horizontal axis is referenced to V⁺ instead. The SD pin should not be set within the voltage range from 1.1V to 1.9V of the selected supply voltage since this is a transition region and the device status will be undetermined.
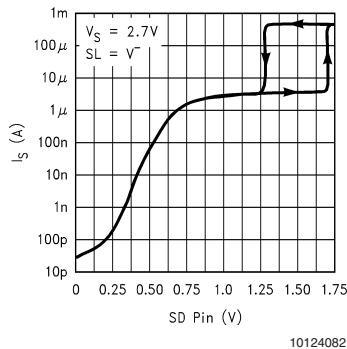


10124082

**FIGURE 1. Supply Current vs. "SD" Voltage**

Table 1, below, summarizes the status of the device when the SL and SD pins are connected directly to V⁻ or V⁺:

**TABLE 1. LMC8101 Status Summary**

| SL | SD | LMC8101 Status |
|----|----|----|
| V⁻ | V⁻ | Shutdown |
| V⁻ | V⁺ | Active |
| V⁺ | V⁺ | Shutdown |
| V⁺ | V⁻ | Active |

In case shutdown operation is not needed, as can be seen in Table 1, the two pins SL and SD can simply be connected to opposite supply nodes to achieve "Active" operation. The SL and SD should always be tied to a node; if left unconnected, these high impedance inputs will float to an undetermined state and the device status will be undetermined as well.

With the device in shutdown, once "Active" operation is initiated, there will be a finite amount of time required before the device output is settled to its final value. This time is less than 15µs. In addition, there may be some output spike during this time while the device is transitioning into a fully operational state. Some applications may be sensitive to this output spike and proper precautions should be taken in order to ensure proper operation at all times.

## TINY PACKAGE

The LMC8101 is available in the micro SMD package as well the 8 pin MSOP package. The micro SMD package requires approximately 1/4 the board area of a SOT23. This package is less than 1mm in height allowing it to be placed in absolute minimum height clearance areas such as cellular handsets, LCD panels, PCMCIA cards, etc. More information about the micro SMD package can be found at: http://www.national.com/appinfo/microsmd.

## CONVERSION BOARDS

In order to ease the evaluation of tiny packages such as the micro SMD, there is a conversion board (LMC8101CONV) available to board designers. This board converts a micro SMD device into an 8 pin DIP package (see *Figure 2*, Conversion Board Pin out diagram) for easier handling and evaluation. This board can be ordered from National Semiconductor by contacting http://www.national.com .



10124089
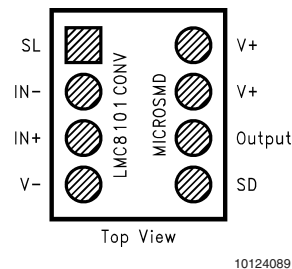
**FIGURE 2. micro SMD Conversion Board pin-out**

## INCREASED OUTPUT CURRENT

Compared to the LMC7101, the LMC8101 has an improved output stage capable of up to three times larger output sourcing and sinking current. This improvement would allow a larger output voltage swing range compared to the LMC7101 when connected to relatively heavy loads. For lower supply voltages this is an added benefit since it increases the output swing range. For example, the LMC8101 can typically swing 2.5Vpp with 2mA sourcing and sinking output current (Vs = 2.7V) whereas the LMC7101 output swing would be limited to 1.9Vpp under the same conditions. Also, compared to the LMC7101 in the SOT23 package, the LMC8101 can dissipate more power because both the MSOP and the micro SMD packages have 40% better heat dissipation capability.

## LOWER 1/f NOISE

The dominant input referred noise term for the LMC8101 is the input noise voltage. Input noise current for this device is of no practical significance unless the equivalent resistance it looks into is 5MΩ or higher.

The LMC8101's low frequency noise is significantly lower than that of the LMC7101. For example, at 10Hz, the input referred spot noise voltage density is 85 nV $\sqrt{Hz}$ as compared to about 200nV $\sqrt{Hz}$ for the LMC7101. Over a frequency range of 0.1Hz to 100Hz, the total noise of the LMC8101 will be approximately 60% less than that of the LMC7101.

# Application Notes (Continued)

### LOWER THD

When connected to heavier loads, the LMC8101 has lower THD compared to the LMC7101. For example, with 5V supply at 10KHz and 2Vpp swing (Av = –2), the LMC8101 THD (0.2%) is 60% less than the LMC7101's. The LMC8101 THD can be kept below 0.1% with 3Vpp at the output for up to 10KHz (refer to the Typical Characteristics Plots).

### IMPROVING THE CAP LOAD DRIVE CAPABILITY

This can be accomplished in several ways:

- Output resistive loading increase:

The Phase Margin increases with increasing load (refer to the Typical Characteristics Plots). When driving capacitive loads, stability can generally be improved by allowing some output current to flow through a load. For example, the cap load drive capability can be increased from 8200pF to 16000pF if the output load is increased from 5kΩ to 600Ω ($A_V$ = +10, 25% overshoot limit, 10V supply).

- Isolation resistor between output and cap load:

This resistor will isolate the feedback path (where excessive phase shift due to output capacitance can cause instability) from the capacitive load. With a 10V supply, a 100Ω isolation resistor allows unlimited capacitive load without oscillation compared to only 300pF without this resistor ($A_V$ = +1).

- Higher supply voltage:

Operating the LMC8101 at higher supply voltages allows higher cap load tolerance. At 10V, the LMC8101's low supply voltage cap load limit of 300pF improves to about 600pF ($A_V$ = +1).

- Closed loop gain increase:

As with all Op Amps, the capacitive load tolerance of the LMC8101 increases with increasing closed loop gain. In applications where the load is mostly capacitive and the resistive loading is light, stability increases when the LMC8101 is operated at a closed loop gain larger than +1.

## Ordering Information

| Package | Part Number | Package Marking | Transport Media | NSC Drawing |
|---|---|---|---|---|
| 8-Bump micro SMD **Leaded** | LMC8101BP | A | 250 Units Tape and Reel | BPA08FFB |
| | LMC8101BPX | 2 | 3k Units Tape and Reel | |
| 8-Bump micro SMD **Lead Free** | LMC8101TP | A | 250 Units Tape and Reel | TPA08FFA |
| | LMC8101TPX | 08 | 3k Units Tape and Reel | |
| 8-Pin MSOP | LMC8101MM | A11 | 1k Units Tape and Reel | MUA08A |
| | LMC8101MMX | | 3.5k Units Tape and Reel | |

# Physical Dimensions   inches (millimeters) unless otherwise noted

SYMM ℄

8X ∅ 0.17 / 0.15

SYMM ℄

(0.5)

(0.5)

**LAND PATTERN RECOMMENDATION**

TOP SIDE COATING

BUMP A1 CORNER

**DIMENSIONS ARE IN MILLIMETERS**
DIMENSIONS IN ( ) FOR REFERENCE ONLY

X3

0.125 / 0.050

C

BUMP

SILICON

0.15 / 0.11

8X ∅ 0.18 / 0.16

⊕ 0.005 Ⓢ C AⓈ BⓈ

B

X2

SYMM ℄

3

2

SYMM ℄

0.5

1

C   B   A

0.5

X1

A

BPA08XXX (Rev D)
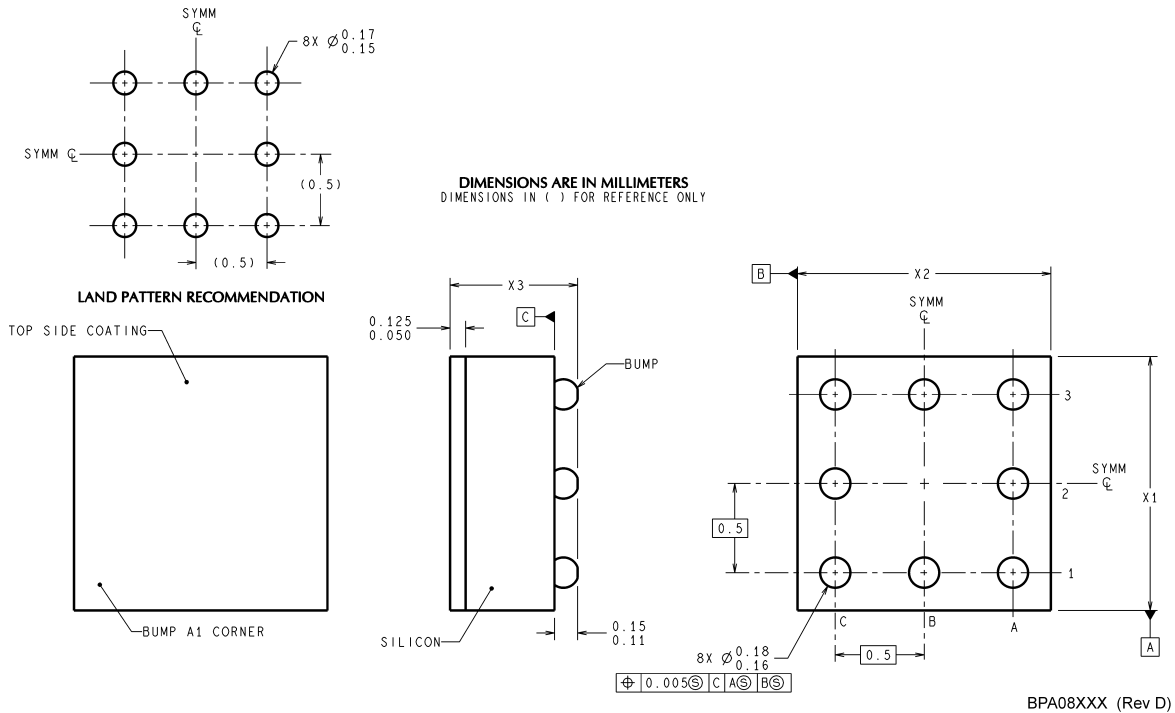
NOTES: UNLESS OTHERWISE SPECIFIED

1. EPOXY COATING

2. 63Sn/37Pb EUTECTIC BUMP

3. RECOMMENDED NON-SOLDER MASK DEFINED LANDING PAD.

4. PIN A1 IS ESTABLISHED BY LOWER LEFT CORNER WITH RESPECT TO TEXT ORIENTATION. REMAINING PINS ARE NUMBERED COUNTERCLOCKWISE.

5. XXX IN DRAWING NUMBER REPRESENTS PACKAGE SIZE VARIATION WHERE X1 IS PACKAGE WIDTH, X2 IS PACKAGE LENGTH AND X3 IS PACKAGE HEIGHT.

6. REFERENCE JEDEC REGISTRATION MO-211, VARIATION BC.

**8-Bump micro SMD Package**
**Order Package Number LMC8101BP, LMC8101BPCONV or LMC8101BPX**
**NS Package Number BPA08FFB**
**$X_1$ = 1.412   $X_2$ = 1.412   $X_3$ = 0.850**

## Physical Dimensions inches (millimeters) unless otherwise noted (Continued)

SYMM
℄

8X Ø 0.17 / 0.15

SYMM ℄

(0.5)

(0.5)

**LAND PATTERN RECOMMENDATION**

TOP SIDE COATING

BUMP A1 CORNER

**DIMENSIONS ARE IN MILLIMETERS**
DIMENSIONS IN ( ) FOR REFERENCE ONLY

X3

0.125 / 0.050

C

BUMP

SILICON

0.15 / 0.11

B

X2

SYMM ℄

3

2  SYMM ℄  X1

0.5

1

8X Ø 0.18 / 0.16

C  B  A

0.5

⊕ 0.005Ⓢ C AⓈ BⓈ

A

TPA08XXX (Rev B)
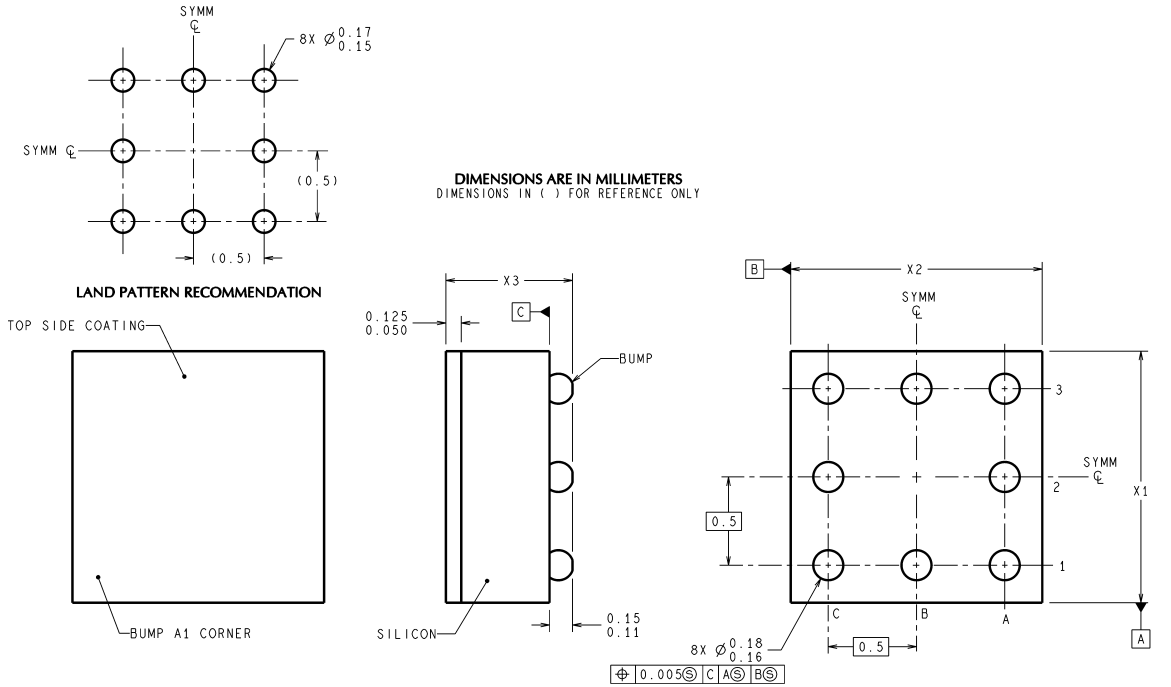
NOTES: UNLESS OTHERWISE SPECIFIED

1. EPOXY COATING

2. FOR SOLDER BUMP COMPOSITION, SEE "SOLDER INFORMATION". IN THE PACKAGING SECTION OF THE NATIONAL SEMICONDUCTOR WEB PAGE (www.national.com)
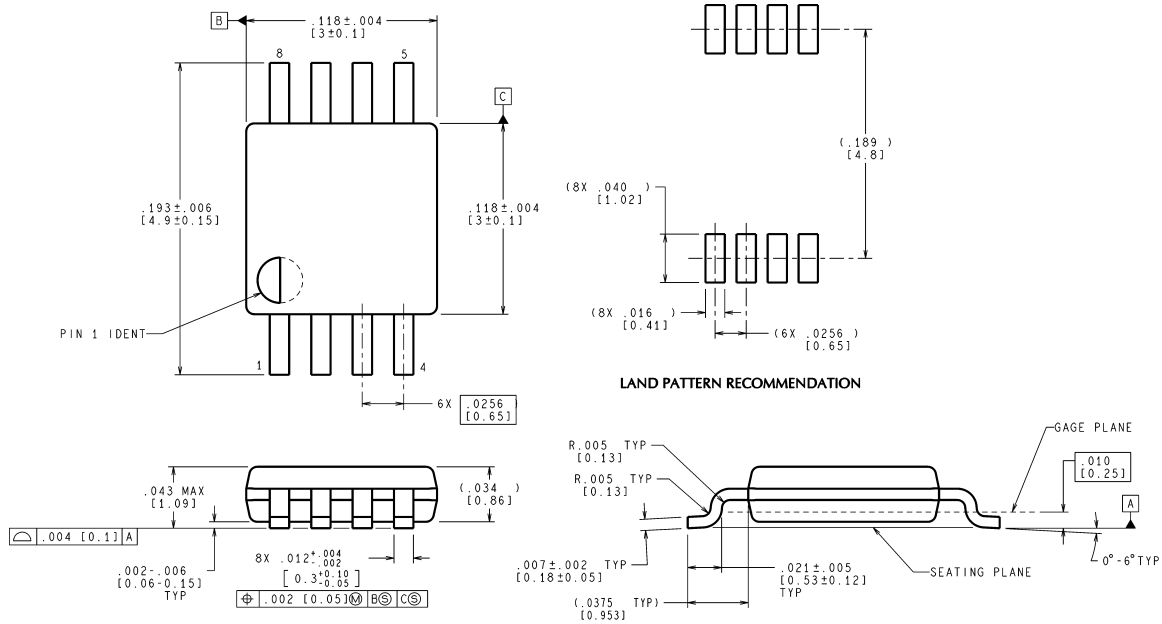
3. RECOMMENDED NON-SOLDER MASK DEFINED LANDING PAD.

4. PIN A1 IS ESTABLISHED BY LOWER LEFT CORNER WITH RESPECT TO TEXT ORIENTATION.

5. XXX IN DRAWING NUMBER REPRESENTS PACKAGE SIZE VARIATION WHERE X1 IS PACKAGE WIDTH, X2 IS PACKAGE LENGTH AND X3 IS PACKAGE HEIGHT.

6. REFERENCE JEDEC REGISTRATION MO-211, VARIATION BC.

**8-Bump micro SMD (Lead Free) Package**
**Order Package Number LMC8101TP, or LMC8101TPX**
**NS Package Number TPA08FFA**
**$X_1$ = 1.412 mm   $X_2$ = 1.412 mm   $X_3$ = 0.5 mm**

# Physical Dimensions inches (millimeters) unless otherwise noted (Continued)

.118±.004
[3±0.1]

.193±.006
[4.9±0.15]

.118±.004
[3±0.1]

PIN 1 IDENT

6X .0256
[0.65]

(.189 )
[4.8]

(8X .040 )
[1.02]

(8X .016 )
[0.41]

(6X .0256 )
[0.65]

**LAND PATTERN RECOMMENDATION**

.043 MAX
[1.09]

.004 [0.1] A

.002-.006
[0.06-0.15]
TYP

8X .012 +.004
           -.002
[ 0.3 +0.10
      -0.05 ]

.002 [0.05] M B S C S

(.034 )
[0.86]

R.005 TYP
[0.13]

R.005 TYP
[0.13]

.007±.002 TYP
[0.18±0.05]

(.0375 TYP)
[0.953]

.021±.005
[0.53±0.12]
TYP

GAGE PLANE

.010
[0.25]

SEATING PLANE

0°-6° TYP

**CONTROLLING DIMENSION IS INCH
VALUES IN [ ] ARE MILLIMETERS**

MUA08A (Rev E)

**8-Pin MSOP Package
Order Package Number LMC8101MM or LMC8101MMX
NS Package Number MUA08A**

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2. A critical component is any component of a life support device or system whose failure to perform can be reasonably expected to cause the failure of the life support device or system, or to affect its safety or effectiveness.

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